Claims 1-17 and 19 stand provisionally rejected over claims in co-pending patent application serial no. 09/408,807. A terminal disclaimer is enclosed herewith to remove that rejection.

Claims 1 and 6-7 stand rejected as being anticipated by Chin et al., U. S. Patent No. 6,286,083.

The claims point out include:

> a data rebuffering section adapted to couple data from a one of a plurality of bi-directional data ports **to a bi-directional data port of the microprocessor** selectively in accordance with a control signal; (emphasis added)

Thus, a plurality of bi-directional ports may be coupled to a port of the microprocessor.

Referring to FIG. 2 of Chin et al. it appears that only the memory bus 110 is coupled to the CPU bus 108.

The Examiner points to column 7, lines 22-40, presented below:

> Referring still to FIG. 2, the CPU interface 210, PCI interface 220, and AGP interface 230 generally ***originate all of the memory read*** requests. Specifically, the CPU interface 210 generates the M2P and M2PG requests, the PCI interface 220 generates the M2I requests, and the AGP interface 230 generates the M2G, M2GI, and M2GART requests. When one of the interfaces 210, 220, or 230 asserts a memory read request, the memory controller 200 submits the associated target addresses for the read request ***to main memory 106***. In response, main memory 106 places the read data into the queue connected between the memory controller 200 and the particular interface originating the read request Thus, M2P and M2PG data are placed in the M2P queue 252, data for the M2I requests are stored the M2I queue 262, and data for the M2G, M2G, and M2GART requests are placed in the M2G queue 272.
>
> The interfaces 210, 220, and 230 also supply the addresses and data for write transactions ***to main memory***. ***The CPU interface 210 provides P2M addresses and data, which are stored in the P2M queue 250 until granted memory access***. Likewise, the I2M queue 260 stores the I2M requests submitted by the PCI interface 220, and the G2M queue 270 stores the G2M

and GI2M requests submitted by the AGP interface 230. The main memory 106 processes write transactions by dequeuing the data and addresses directly from the queues 250, 260, and 270. The refresh request preferably is generated by the memory controller 200, as described in greater detail with respect to FIG. 3D (emphasis added).

Thus, it is respectfully submitted that Chin et al does not describe a data rebuffering section adapted to couple data from a one of a plurality of bi-directional data ports **to a bi-directional data port of the microprocessor** selectively in accordance with a control signal.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Date

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